Unit 22

Answers: Semiconductor Devices

Quick checks

1 b The carriers near the junction have diffused across and recombined. What remains are the ions that can't move: on the p side the acceptor ions, which took an electron each and are negative; on the n side the donor ions, which gave one away and are positive.

2 a The n side of the layer is positive (donor ions) and the p side negative (acceptor ions), and a field points from + to −. It pushes holes back to the p side and electrons back to the n side, which is why diffusion stops.

3 b It conducts when forward biased: p side (anode) to +. And for silicon the applied voltage must be more than the barrier, about 0.7 V, before a sizeable current flows.

4 b The reverse current is carried by minority carriers, made by heat at a fixed rate; even at a few volts all of them are already swept across. A larger voltage has no more carriers to move, so the current hardly changes until breakdown. A diode doesn't obey Ohm's law.

5 a D_1 has 5 V on its anode, and its cathode is joined to earth through R: it is forward biased, conducts, and lifts Y to 5 V, a 1. D_2's anode is at 0 V and its cathode now at Y = 5 V: it is reverse biased.

6 c That is the NAND table: 1, 1, 1, 0. An AND gate is the opposite (1 only when both are 1); a NOR gate is 0 whenever any input is 1.

7 b The barrier potential is made by the fixed ions on the two sides of the **depletion layer**, and it is across that layer.

8 b Reverse biased, the majority carriers are pulled away from the junction; only a tiny current of minority carriers flows. ("Positive" and "negative" bias are not terms used for diodes.)

9 b In reverse bias the depletion layer is **wide**, the resistance **very high**, and the current almost zero (a few μA of minority carriers).

10 b A **rectifier** converts a.c. into d.c. It is made of diodes, but a single diode on its own is only its part; a transformer changes the size of an a.c. voltage, not its kind.

11 b Working in reverse breakdown, the voltage across a Zener diode stays at V_Z over a wide range of currents, so it holds a voltage steady: a **voltage regulator**.

12 d NAND (like NOR) is a **universal gate**: NOT, AND and OR can all be made of NAND gates alone. OR, AND or NOT gates on their own can't make every gate.

13 a One NAND gate with its two inputs joined: $\overline{A \cdot A} = \bar{A}$.

14 a The first NOR gives $\overline{A + B}$; the second, with its inputs joined, inverts it: $\overline{\overline{A + B}} = A + B$, an **OR gate**.

15 d The NOR gate with both inputs equal to A + B gives $\overline{A + B}$: the whole circuit is a **NOR gate** (Example 22.6).

16 a Boolean algebra is the algebra of **logic**: of statements that are either true or false, combined with AND, OR and NOT.

11.

a. In the p region the majority carriers are holes, in the n region free electrons. Because of the difference in their concentrations, holes **diffuse** from the p side into the n side and electrons from the n side into the p side, where they **recombine**. So a thin region on each side of the junction (about 0.01–1 μm) is left with no free carriers: the **depletion layer**. It contains only the fixed ions: negative acceptor ions on the p side, positive donor ions on the n side. These charges set up an **electric field** from the n side to the p side, which opposes further diffusion; diffusion stops when the two balance. The potential difference across the depletion layer is the **potential barrier**: about 0.7 V for silicon and 0.3 V for germanium.

b. **Forward characteristic** (p side to +; circuit Figure 22.4): as the forward voltage rises from zero, almost no current flows until the barrier is overcome, at the knee voltage (0.7 V for Si, 0.3 V for Ge). Beyond the knee the current (in mA) rises very steeply, since the depletion layer is thin and the resistance low. Too large a current overheats and destroys the diode.

Reverse characteristic (p side to −, with a microammeter; Figure 22.6): only a tiny reverse current of minority carriers flows (μA), almost constant as the voltage rises, since the depletion layer is wide and the resistance very high. At the **breakdown voltage** V_B the current suddenly rises sharply, as carriers accelerated by the strong field knock more electrons out of their bonds (avalanche). The graph is Figure 22.5.

12. a. A **junction diode** is a p–n junction with a lead to each side: it lets current through when forward biased and practically none when reverse biased.
Full-wave rectifier with two diodes (Figure 22.10): the secondary of a center-tapped transformer has ends S_1 and S_2; S_1 goes through diode D_1 and S_2 through D_2 to one end (X) of the load R_L; the center tap goes to the other end (Y). In one half cycle S_1 is positive with respect to the center tap: D_1 conducts, D_2 is reverse biased, and current flows $S_1 \rightarrow D_1 \rightarrow X \rightarrow R_L \rightarrow Y \rightarrow$ center tap. In the next half cycle S_2 is positive: D_2 conducts, D_1 is off, and current flows $S_2 \rightarrow D_2 \rightarrow X \rightarrow R_L \rightarrow Y$. In both halves the current through R_L flows from X to Y, so both halves of the a.c. give output in the same direction (Figure 22.12).

b. If one diode fails **open** (it no longer conducts), the circuit works on only one half of each cycle: it becomes a **half-wave rectifier**, with half the average output and a gap every other half cycle. If a diode fails **short-circuited**, then in the half cycle when it should be blocking, it joins its end of the secondary straight to the other end through the working diode, short-circuiting the transformer: a very large current flows, which can damage the transformer and the other diode (or blow a fuse).

c. A **Zener diode** (after a filter capacitor), connected reverse biased across the load with a series resistor (Figure 22.8), gives a constant output voltage V_Z. Its symbol and characteristic are Figure 22.3 and Figure 22.7: forward like an ordinary diode; reverse, almost no current until V_Z, then a nearly vertical rise at constant voltage.

13. a. **Logic gates** are digital circuits with one or more inputs and one output, each either 1 (high voltage) or 0 (low voltage), whose output follows a definite logical rule of the inputs (OR, AND, NOT, and combinations). They are the building blocks of computers and other digital systems.
The **NAND gate** is an AND gate followed by a NOT; its symbol is the AND symbol with a small circle at its output (Figure 22.20), and $Y = \overline{A \cdot B}$:

A	B	Y = $\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

b. The NAND gate is **universal** because NAND gates alone can make the three basic gates, and so any logic circuit (Figure 22.21):

- NOT: one NAND with its inputs joined, $\overline{A \cdot A} = \bar{A}$;
- AND: a NAND followed by a NAND-NOT, $\overline{\overline{A \cdot B}} = A \cdot B$;
- OR: $\bar{A}$ and $\bar{B}$ from two NAND-NOTs into a third NAND, $\overline{\bar{A} \cdot \bar{B}} = A + B$.

14. a. Two NOR gates with their inputs joined give $\bar{A}$ and $\bar{B}$; a third NOR gives

$$Y = \overline{\bar{A} + \bar{B}} = A \cdot B$$

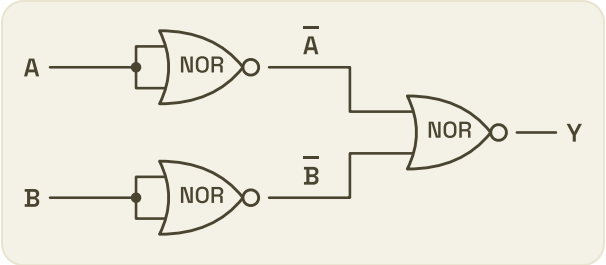


Figure 22.32 *An AND gate made of three NOR gates.*

A	B	$\bar{A}$	$\bar{B}$	$\bar{A} + \bar{B}$	Y
0	0	1	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	0	1

b. A NOT gate after an AND gives $\overline{A \cdot B}$: a **NAND gate**.

c. The first NAND gate, with both inputs A, gives $\bar{A}$; the second gives $\bar{B}$; the third gives $Y = \overline{\bar{A} \cdot \bar{B}}$.

A	B	$\bar{A}$	$\bar{B}$	$\bar{A} \cdot \bar{B}$	Y
0	0	1	1	1	0
0	1	1	0	0	1
1	0	0	1	0	1
1	1	0	0	0	1

The output column, 0 1 1 1, is exactly that of A + B: the circuit acts as an **OR gate**.