Unit 4 · From Code to Circuits

ANSWER KEY · FOR TEACHERS

Full marks 33

Give the marks for the points in the marking scheme; an answer in other words that says the same is right.

1 Key words

K · 4

1. registers
2. program counter
3. opcode
4. mask
5. flip-flop
6. compiler
7. scheduler
8. threads

Each carries 0.5 mark.

2 Label the diagram

U · 2

1. Ready
2. its time slice is over
3. Waiting
4. Running

Each carries 0.5 mark.

3 Multiple choice

i. **b.** SUB R2, #1 — A · 1

The first digit, 7, is the opcode of SUB with a number; the second, 2, is the register R2; the last two, 01, are the number. ADD with a number would be 5, STORE 3.

ii. **c.** 40 — A · 1

A logical shift left by 3 moves every bit 3 places left, with 0s coming in on the right: 0010 1000, which is 40. Each place left doubles the number, so 3 places multiply it by $2^3 = 8$, and $5 \times 8 = 40$.

iii. **b.** instructions and data sharing one path to memory, so they must take turns on it — K · 1

In the Von Neumann design one memory holds both, and one bus carries an instruction or a number at a time, so fetching the next instruction waits while data is moved. The Harvard design gives each its own memory and path.

iv. **b.** 3 — A · 1

Sign 0: positive. Exponent 1000 = 8, 8 − 7 = 1. Mantissa 1.100 in binary = 1.5. So $1.5 \times 2^1 = 3$.

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4 Trace the program

ANSWER **A · 4**

R0	R1	Flag	Output
4	3	greater	
7	2	greater	
9	1	greater	
10	0	equal	
			10

ii. **20**: the two MOVs, then ADD, SUB, CMP and BGT four times round the loop (16), then OUT and HALT. The program adds 4 + 3 + 2 + 1.

MARKING SCHEME

- ✓ R0 4, 7, 9, 10 (each time R1 added to it).
- ✓ R1 3, 2, 1, 0, with the flag greater, greater, greater, equal.
- ✓ The loop ends when the flag says equal, and OUT shows 10.
- ✓ 20 instructions.

5 Masks

MARKING SCHEME **A · 3**

- ✓ i. The inverter is charging and the battery is low (bits 1 and 2); it is not on battery and there is no overload.
- ✓ ii. OR with 0000 1000, giving 0000 1110.
- ✓ iii. AND with 1111 1011, giving 0000 0010.

6 Write a program

ANSWER **A · 4**

Address	Assembly	Machine code
0	`MOV R0, #2`	1002
1	`loop: OUT R0`	F003
2	`ADD R0, #2`	5002
3	`CMP R0, #12`	900C
4	`BLT loop`	D001
5	`HALT`	0000

The output is 2 4 6 8 10: after 10 is shown, R0 becomes 12, the flag says equal, and BLT isn't taken. Also right: `CMP R0, #10` with `BGT done` and `B loop`, or `CMP R0, #11` with `BLT loop`, each with its own machine code.

MARKING SCHEME

- ✓ A loop that shows R0 and adds 2 to it, starting from 2.
- ✓ A compare and branch that stop it after 10 is shown, and HALT.
- ✓ Machine code of MOV, OUT and ADD right (1002, F003, 5002).
- ✓ Machine code of the compare, the branch (with the loop's address) and HALT right (900C, D001, 0000).

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7 Taking turns

ANSWER **A · 4**

Process	Arrives	Needs	FCFS finishes	FCFS waits	SJF finishes	SJF waits
P	0	5	5	0	5	0
Q	1	2	7	4	8	5
R	2	6	13	5	14	6
S	3	1	14	10	6	2

i. FCFS runs P 0–5, Q 5–7, R 7–13, S 13–14. Average waiting time = (0 + 4 + 5 + 10) ÷ 4 = **4.75 ms.**

ii. SJF: only P is ready at 0, so it runs to 5. Then the shortest ready job each time: S 5–6, Q 6–8, R 8–14. Average = (0 + 5 + 6 + 2) ÷ 4 = **3.25 ms.**

MARKING SCHEME

✓ FCFS finishing times 5, 7, 13, 14.

✓ FCFS average 4.75 ms.

✓ SJF order P, S, Q, R (P not stopped, because SJF is non-preemptive).

✓ SJF average 3.25 ms.

8 Simplify the circuit

ANSWER **A · 3**

i. A·B is used twice (idempotent: A·B + A·B = A·B):

L = ($\overline{A}$·B + A·B) + (A·$\overline{B}$ + A·B)

= B·($\overline{A}$ + A) + A·($\overline{B}$ + B) (distributive)

= B·1 + A·1 (complement)

= A + B (identity)

So the light is on when A or B is on: one OR gate instead of three ANDs, an OR and two NOTs.

ii. NOT (A + B) = $\overline{A}$·$\overline{B}$: the light is off only when A and B are both off.

MARKING SCHEME

✓ The terms grouped so each pair shares a letter (A·B used twice, idempotent; or X + $\overline{X}$·Y = X + Y).

✓ The rules named and used right: distributive, complement, identity.

✓ L = A + B.

9 A float in 8 bits

ANSWER **A · 3**

i. 6.5 = 110.1 in binary = 1.101×2^2. The exponent 2 + 7 = 9 = 1001; the mantissa is the bits after the point, 101. So **0 1001 101.**

ii. Sign 1: negative. Exponent 1001 = 9, minus 7 = 2. Mantissa 1.010 = 1.25. So -1.25×2^2 = **−5.**

iii. 0.1 = 1/10, and 10 has a factor 5. In binary it goes on for ever (0.000110011…), as 1/3 does in decimal, so any number of bits must cut it off. The format stores the nearest value it can (0.1015625 in 8 bits).

MARKING SCHEME

✓ 0 1001 101.

✓ −5.

✓ 0.1 in binary repeats for ever (its denominator, 10, isn't a power of 2), so it is rounded to the nearest value the bits can hold.

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10 Think

ANSWER HA · 2

Thread 1 loads 5 into its register. Before it stores, thread 2 also loads 5. Thread 1 adds 1 and stores 6; thread 2 adds 1 to its own 5 and stores 6 too. One addition is lost, because each thread's three steps can be split by a switch to the other thread: a race condition. The fix is a lock (a mutex): a thread takes the lock before its LOAD and lets go after its STORE, so the other must wait, and the three steps always run together.

MARKING SCHEME

- ✓ An order in which both threads LOAD 5 before either STOREs, so both store 6 and one addition is lost.
- ✓ A lock round the LOAD, ADD and STORE, so only one thread at a time can do them.

11 Activity: Four ways to choose

(not marked)

WHAT STUDENTS SHOULD FIND

The averages are 6 ms (FCFS), 5.25 ms (SJF), 3.5 ms (SRT) and 6.5 ms (round robin). Running the short jobs first gives the lowest averages, but long A waits 10 ms under SRT, the longest of any rule. With **Short jobs keep coming**, SJF and SRT starve the long jobs, while FCFS and round robin finish every job.

Marks by level	Knowledge	Understanding	Application	Higher ability	**Total**
Marks	5	2	24	2	**33**

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